60. The method of claim 41, wherein depositing the low k dielectric material comprises introducing a processing gas including trimethylsilane to a processing chamber at a flow rate of about 175 sccm, introducing an oxidizing gas at a flow rate of about 5000 sccm, introducing an inert gas into the processing chamber at a rate of about 8000 sccm, maintaining a chamber pressure of about 100 Torr, and maintaining a substrate surface temperature of about 125°C.

REMARKS

This is intended as a full and complete response to the Office Action dated November 21, 2002, having a shortened statutory period for response set to expire on February 21, 2003. Claims 1-60 are pending in the application. Claims 1-60 were considered by the Examiner and stand rejected. Applicants believe that no new matter has been introduced in this response.

Claims 1-60 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Bjorkman et al.* (U.S. Patent No. 6,340,435) in view of *Yau et al.* (U.S. Patent No. 6,054,379). The Examiner asserts that it would have been obvious to modify *Bjorkman* by removing a portion of the remaining dielectric layer in order to deposit a new, low k dielectric layer and self-planarizing layer as taught by *Yau*. Applicants respectfully respond to this rejection.

The *Bjorkman et al.* reference cited by the Examiner and the present application were commonly owned by Applied Materials, Inc., at the time the invention of the present application was made. Applicants have enclosed a statement of common ownership regarding the *Bjorkman et al.* reference. Thus, *Bjorkman et al.* is not a reference for use in a rejection under §102(e)/103(a).

Alternatively, the combination of *Bjorkman et al.* and *Yau et al.* does not teach, show, or suggest the subject matter of claims 1-60. *Bjorkman et al.* discloses a method of depositing and etching dielectric layers having low dielectric constants and etch rates that vary by at least 3:1 for the formation of feature definitions. *Yau et al.* discloses depositing an oxidized organo silane film from an organo silane compound and an

oxidizing gas as a liner layer, cap layer, etch stop or intermetal dielectric layer, which layers may be etched to form feature definitions when necessary.

The combination of *Bjorkman et al.* and *Yau et al.* does not teach, show, or suggest depositing one or more conductive materials to fill at least a portion of a feature definition, planarizing the one or more conductive materials to expose the dielectric material, removing at least a portion of the dielectric material, and depositing a low k dielectric material, as recited in claim 1 and claims dependent thereon.

The combination of *Bjorkman et al.* and *Yau et al.* does not teach, show, or suggest depositing a conductive barrier layer over exposed surfaces of a dual damascene definition, depositing a conductive material over the conductive barrier layer to fill at least a portion of the dual damascene definition, planarizing the conductive barrier layer and the conductive material to expose the one or more dielectric layers, removing at least a portion of the one or more dielectric layers, depositing a low k dielectric material, and depositing a self-planarizing dielectric layer on the low k dielectric material, as recited in claim 25 and claims dependent thereon.

The combination of *Bjorkman et al.* and *Yau et al.* does not teach, show, or suggest depositing a conductive barrier layer over exposed surfaces of the dual damascene definition, depositing a conductive material over the conductive barrier layer to fill at least a portion of the dual damascene definition, planarizing the conductive barrier layer and the conductive material to expose the one or more dielectric layers, removing the one or more dielectric layers, depositing a low k dielectric material on the substrate, and depositing a self-planarizing dielectric layer on the low k dielectric material, as recited in claim 41 and claims dependent thereon.

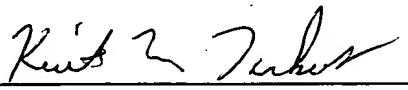
Withdrawal of the rejection to claims 1-60 is respectfully requested.

The prior art made of record is noted. However, it is believed that the secondary references are no more pertinent to the Applicants' disclosure than the primary references cited in the office action. Therefore, it is believed that a detailed discussion of the secondary references is not deemed necessary for a full and complete response to this office action. Accordingly, allowance of the claims is respectfully requested.

In conclusion, the references cited by the Examiner, neither alone nor in combination, teach, show, or suggest the claimed aspects of the invention. Having

addressed all issues set out in the office action, applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A method for processing a substrate, comprising:

(a) forming a feature definition in a dielectric material deposited on a surface of a substrate;

(b) depositing one or more conductive materials to fill at least a portion of the feature definition;

(c) planarizing the [substrate surface] one or more conductive materials to expose the dielectric material;

(d) removing at least a portion of the dielectric material; and

(e) depositing a low k dielectric material.

2. (Amended) The method of claim 1, wherein forming a feature definition in a dielectric material comprises:

(a) depositing a first dielectric material;

(b) depositing a second dielectric material on the first dielectric material;

(c) depositing a third dielectric layer on the second dielectric material;

(d) etching the first, [and] second, and third dielectric layers to form a vertical interconnect; and

(e) etching the third dielectric layer to form a horizontal interconnect.

20. (Amended) The method of claim 1, wherein planarizing the [substrate surface] one or more conductive materials comprises chemical mechanical polishing the [substrate surface] one or more conductive materials.

25. (Amended) A method for forming a dual damascene interconnect, comprising:

(a) depositing one or more dielectric layers on a substrate;

(b) etching the one or more dielectric layers to form a dual damascene definition therein, the dual damascene definition having a vertical interconnect and a horizontal interconnect;

(c) depositing a conductive barrier layer over exposed surfaces of the dual damascene definition;

(d) depositing a conductive material over the conductive barrier layer to fill at least a portion of the dual damascene definition;

(e) planarizing [the filled dual damascene definition] the conductive barrier layer and the conductive material to expose the one or more dielectric layers;

(f) removing at least a portion of the one or more dielectric layers;

(g) depositing a low k dielectric material; and

(h) depositing a self-planarizing dielectric layer on the low k dielectric material.

41. (Amended) A method for forming a dual damascene interconnect, comprising:

(a) depositing a first dielectric material;

(b) depositing a second dielectric material on the first dielectric material;

(c) etching the second dielectric layer to exposed a portion of the first dielectric layer;

(d) depositing a third dielectric layer on the second dielectric material and exposed portion of the first dielectric layer;

(e) etching the first and third dielectric layers to form a vertical interconnect and a horizontal interconnect of a dual damascene definition;

(f) depositing a conductive barrier layer over exposed surfaces of the dual damascene definition;

(g) depositing a conductive material over the conductive barrier layer to fill at least a portion of the dual damascene definition;

(h) planarizing [the filled dual damascene definition] the conductive barrier layer and the conductive material to expose the one or more dielectric layers;

(i) removing the one or more dielectric layers;

(j) depositing a low k dielectric material on the substrate; and

(k) depositing a self-planarizing dielectric layer on the low k dielectric material.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Gaillard, et al.

Serial No.: 09/706,298

Confirmation No.: 6722

Filed: November 3, 2000

For: Novel Integration Scheme for Dual Damascene Structure

§ Group Art Unit: 1765

§ Examiner: V. Perez Ramos

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

CERTIFICATE OF MAILING
37 CFR 1.8
I hereby certify that this correspondence is being deposited on February 20, 2003 with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231.

2/20/03 — Date
Keith M. Tackett — Signature

STATEMENT OF COMMON OWNERSHIP

The present application (Serial No. 09/706,298; hereinafter the "Application") and U.S. Patent No. 6,340,435, *Bjorkman et al.*, were, at the time the invention of the Application was made, owned by the same person, or subject to an obligation of assignment to the same person, Applied Materials, Inc.

Respectfully submitted,

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